SILICON BIPOLAR FIXED AND VARIABLE GAIN AMPLIFIER MMICs FOR MICROWAVE AND LIGHTWAVE APPLICATIONS UP TO 6 GHz

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Abstract: A variety of fixed and variable gain amplifier MMICs for applications up to 6 GHz are presented. The circuits are fabricated using an f_T = 10 GHz, f_{max} = 20 GHz, non-polysilicon-emitter silicon bipolar process. Three amplifier topologies and their performance will be reported: a fixed-gain wideband amplifier, a high-gain low-noise amplifier that can also be effectively used as a transimpedance amplifier and a variable gain amplifier.

Introduction

Wideband amplifiers are needed in almost all modern microwave/lightwave communication and instrumentation systems. Silicon bipolar MMICs offer cost-effective solutions for commercial, industrial and military applications up to 6 GHz such as fiber-optic receivers and repeaters, mobile and satellite receivers, millimeter wave receiver IF amplifiers, and military communication receivers.

This paper presents three practical amplifier topologies. (I) An 8 dB gain, f_{-3dB} = 6 GHz, fixed-gain wideband amplifier, fabricated in a modified discrete transistor process, (II) a high-gain low-noise (1.6 dB) amplifier that can also be effectively used as a transimpedance amplifier, and (III) a wide gain control range (50 dB) 3 GHz variable gain amplifier (VGA) suitable for 5 Gbit/s data rates in digital lightwave systems. The last two MMICs were fabricated using a fully-isolated transistor process.

The MMICs were designed using SPICE, both for the linear and the large-signal time-domain analyses. It is imperative that the transistor models used in the computer simulations be accurate [1]. Fortunately, large-signal models for the bipolar transistor have been available for a long time and its high-frequency characteristics are thoroughly understood. The large signal model used for each transistor is shown in Figure 1. In addition to the intrinsic transistor that simulates the action under the emitter, there is a resistor-diode ladder network to model the distributed characteristic of the extrinsic base, parasitic capacitors and contact resistors. The intrinsic transistor uses the extended unified Gummel-Poon model in SPICE.

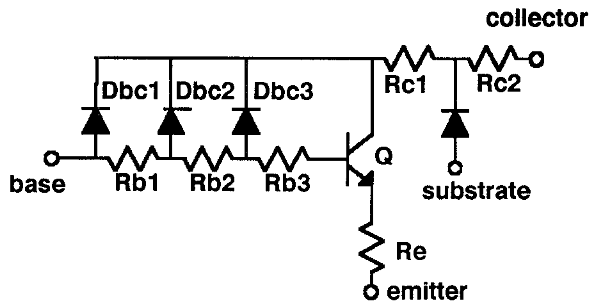

Figure 1. Large-signal transistor model.

Fixed-Gain Wideband Amplifier

The circuit topology of the wideband MMIC (Fig. 2) consists of a Darlington-connected transistor pair with a simple resistive bias network and shunt and series resistive feedback that set the gain and terminal impedances [2]. In order to achieve a 6 GHz bandwidth, a low shunt feedback resistor value is required. Since this resistor also sets the bias of the transistors, there is a practical limit to its lower value. To eliminate this problem, a high resistance path is provided from output to input (R_{FB}) to establish the bias, and a low value resistor (R_F), connected in series with a DC blocking capacitor defines the RF performance. Due to the small die size (.3 mm X .4 mm) and the single supply requirement of the MMIC, the amplifier, including the off-chip blocking capacitor, can be assembled in standard plastic or ceramic microwave transistor packages (Fig. 3).

The MMIC was fabricated using Avantek's SAT f_T = 10 GHz f_{max} = 20 GHz nitride self-aligning process featuring interdigitated 0.6 μm-wide metal-contacted

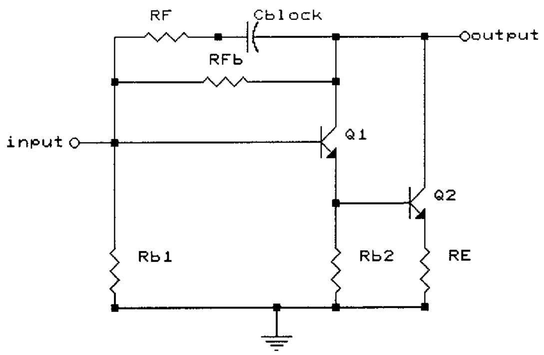

Figure 2. Wideband amplifier equivalent circuit.

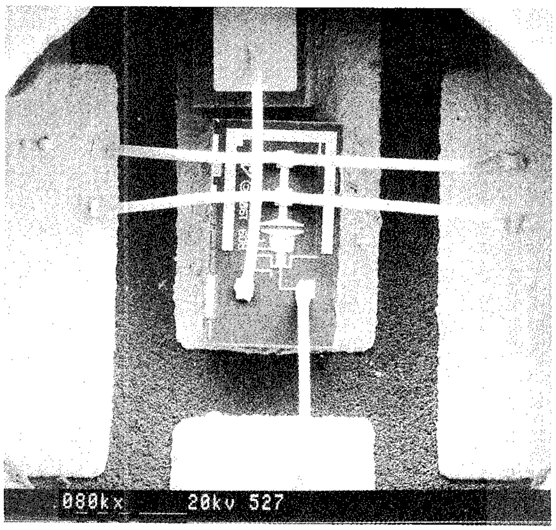

Figure 3. Wideband amplifier, including off-chip blocking capacitor, assembled in 100 mil ceramic microstrip package.

arsenic-doped emitters with 4 μm emitter-to-emitter pitch, 2 μm-thick local oxide isolation, ion implantation, thin-film polysilicon resistors and gold metallization. The MMIC biased at 8 V and 35 mA exhibits (Fig. 4) 8 dB of gain, ± 0.2 dB gain flatness (in the 0.1 to 4.0 GHz band), 3 dB bandwidth of 6 GHz, input and output VSWRs better than 2:1, and 1 GHz noise figure and output compression point of 6 dB and 11.5 dBm respectively.

Fixed-Gain Low-Noise Amplifiers

The circuit topology of the low-noise amplifiers is shown in Fig. 5. The input stage consists of a single transistor driving the output stage which consists of a Darlington pair with local shunt and series feedback. There is also an overall shunt-series feedback loop

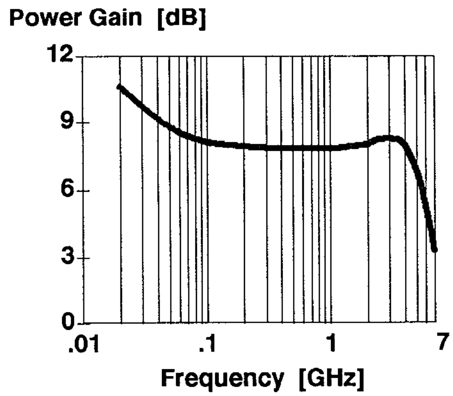

Figure 4. Wideband amplifier. Power gain vs. frequency.

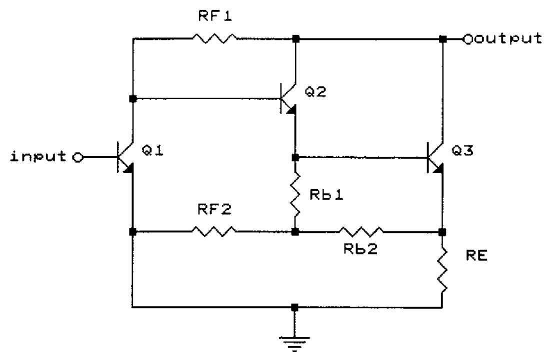

Figure 5. Low-noise amplifier equivalent circuit.

composed of resistors R_E and R_{F2}. Using this topology two high-gain low-noise amplifiers have been fabricated. The measured and simulated performance of the amplifiers is shown in Fig. 6. The INA02 biased at 5.5 V and 35 mA exhibits 32 dB of gain, 1.6 dB noise figure, 3 dB bandwidth of 1 GHz, input and output VSWRs of 1.3:1 and output compression point of 11 dBm. The INA03 biased at 4.5 V and 12 mA exhibits 26 dB of gain, 2.0 dB noise figure, 3 dB bandwidth of 3GHz, input and output VSWRs of 2:1 and 3:1 respectively and output compression point of 1 dBm. The different performance is obtained by varying the size and bias of the transistors and the value of the resistors. For narrowband applications the amplifiers are usable to higher frequencies.

Due to their small die size (.4 mm X .5 mm) and the single supply requirement of the MMICs, the amplifiers can also be assembled in standard microwave transistor packages. The MMICs were fabricated using Avantek's ISOSAT^{TM} process (Fig. 7), which is similar to the above referenced SAT process but produces fully isolated transistors by the use of a global buried layer and deep trench isolation. It also provides a 2nd layer of gold metallization and polyimide passivation.

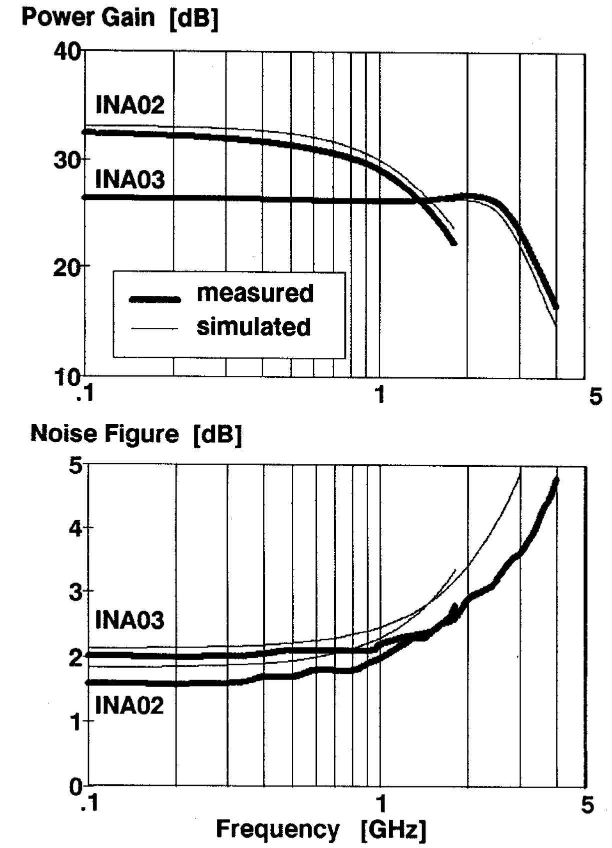

Figure 6. Low-noise amplifiers. Measured and simulated power gain and noise figure vs. frequency.

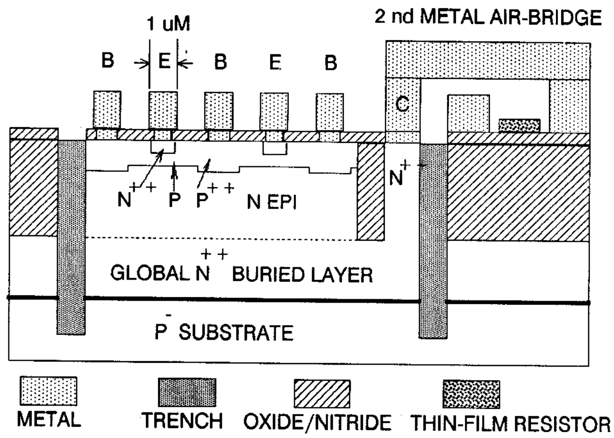

Figure 7. Schematic cross-section of the ISOSAT™ process.

These amplifiers can also be effectively used as low-cost transimpedance amplifiers in digital lightwave systems. The INA02 can be used for data rates up to 800 Mbit/s, having a transimpedance gain of 65 dB and an input current noise spectral density of 6 pA/√Hz. The

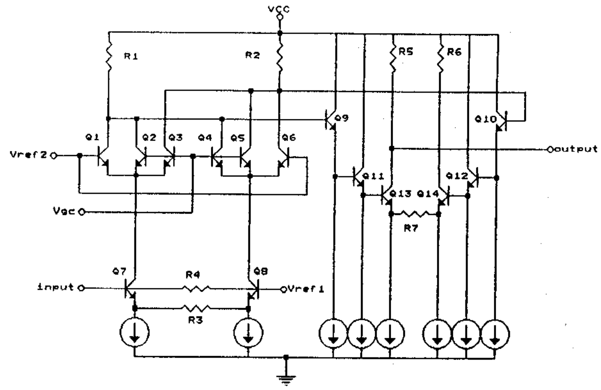

Figure 8. Variable gain amplifier simplified equivalent circuit.

INA03 can be used for data rates in excess of 2.5 Gbit/s, it has a transimpedance gain of 55 dB and an input current noise spectral density of 5 pA/√Hz.

Variable Gain Amplifier

The simplified equivalent circuit of the two stage VGA is shown in Fig. 8. The first stage provides the variable gain mechanism and the second stage acts as a fixed gain output buffer. The circuit is based on the principle of current steering between emitter coupled transistors [3]. For Vgc << Vref2 transistors Q2-Q5 are turned off, transistors Q1 and Q6 act as a cascode and the amplifier exhibits maximum gain. On the other hand, for Vgc >> Vref2 transistors Q1 and Q6 are turned off and the quad Q2-Q5 is on. Since the collectors of the quad are cross-coupled, the amplifier will exhibit maximum loss. The maximum loss is limited by the parasitics of the quad and by the base-emitter voltage (Vbe) mismatch. In general, as Vgc increases the gain decreases monotonically. Emitter-followers Q9-Q12 buffer the loading from the output transistors, Q13-Q14, on the sensitive nodes (collectors of Q1-Q6) and provide level shifting. The input and output terminal impedances are set by resistors R4 and R5 respectively, and are independent of gain.

A microphotograph of the die is shown in Fig. 9. The MMIC was fabricated using the ISOSAT™ process and measures .5 mm X .75 mm. The measured and simulated performance of the amplifier is shown in Fig. 10. Biased at 5.5 V and 40 mA, the device exhibits 24 dB of maximum gain, 3 dB bandwidth of 3.5 GHz, 50 dB gain control range, input and output VSWRs better than 2:1 (at all gain levels), and output compression point and noise figure at maximum gain of -2 dBm and 9 dB respectively. The amplifier has a 300 psec group delay and it changes by less than ± 50 psec over the whole gain control range. This makes it very attractive for digital

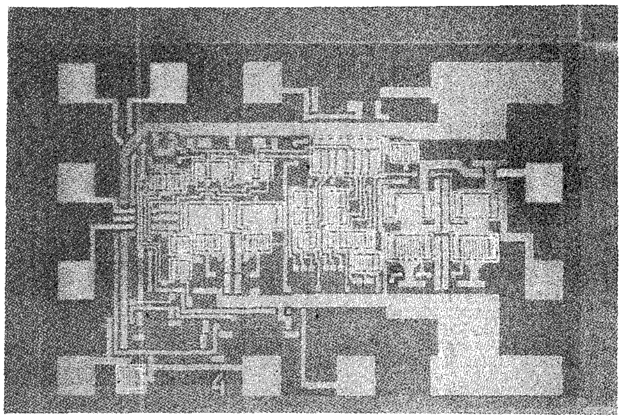

Figure 9. Microphotograph of the variable gain amplifier.

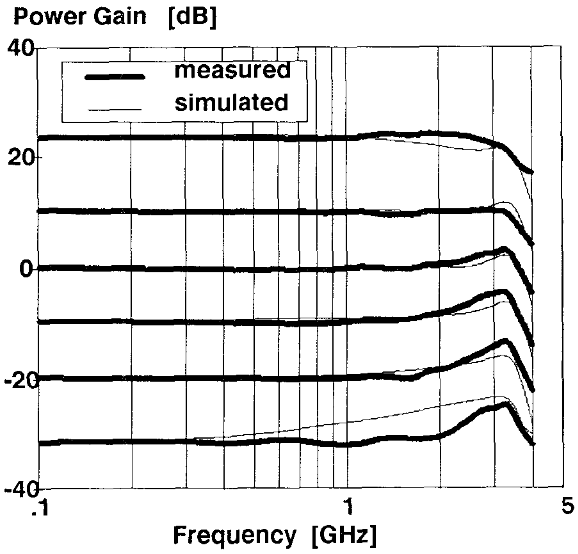

Figure 10. Variable gain amplifier. Measured and simulated power gain vs. frequency.

lightwave applications. Fig. 11 shows the measured (Fig. 11a) and simulated (Fig. 11b) eye diagrams of the output at a 2.5 Gbit/s data rate and the measured (Fig. 11c) eye diagram at a 5 Gbit/s data rate. The measured and simulated performances are from 2^{15}-1 and 2^{5}-1 pseudorandom pattern sources respectively.

Summary and Conclusions

A variety of silicon bipolar fixed and variable gain amplifier circuits have been presented. The circuits were fabricated using Avantek's f_T = 10 GHz f_{max} = 20 GHz, non-polysilicon-emitter silicon bipolar processes. These MMICs, together with some other examples [4],[5], illustrate the capability of silicon bipolar technology to offer cost-effective solutions for microwave applications up to 6 GHz and for digital lightwave applications up to 5

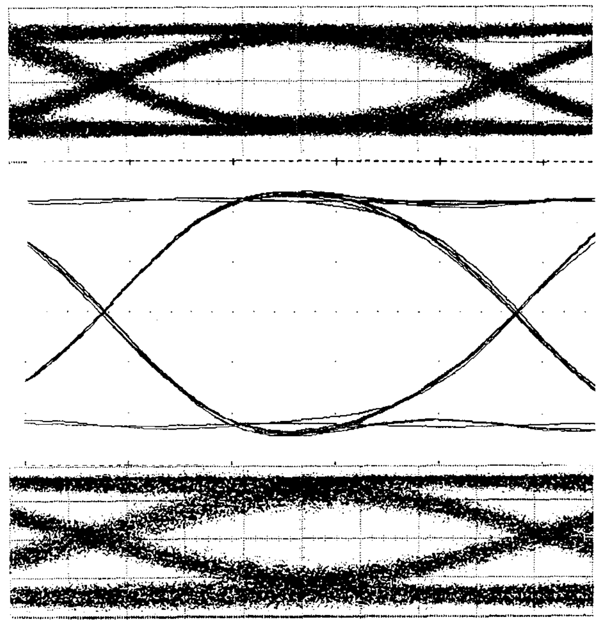

Figure 11. Variable gain amplifier. Measured (a) and simulated (b) eye diagrams at 2.5 Gbit/s, and measured (c) eye diagram at 5 Gbit/s.

Gbit/s. Future scaling of silicon bipolar transistor critical geometries and vertical profiles are expected to extend the useful range in excess of 10 GHz and 10 Gbit/s.

Acknowledgments

The authors wish to thank M. Dutta for her help with wafer processing, and C. Mohr and K. Fischer for their assistance with wafer probing and device characterization.

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